ELEC-374 CPU Laboratory Project

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# Abstract

The ELEC-374 CPU Laboratory Project is a series of laboratory assignments dedicated to the development of a functional Reduced Instruction Set Computer (RISC) Processor. The processor is designed and simulated through the Quartus-II CAD software, and is to be implemented on an Altera DE0 FPGA board. Functionality is to include a datapath, ALU, memory access, and Control Unit, among others.

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# Project Specification

The processor to be designed is

* 32-bit
* 16-bit addresses
* Capable of addressing up to 512(?) bits of memory
* Includes an ALU that can perform the operations Add, Sub, Mul, Div, SHR, SHL, ROR, ROL, OR, AND, NEG, NOT
* Includes several memory operations: Load, Store, Load Imm/ext, store ext, NOP, HALT
* (break down opcodes here, i.e. which bits mean which)
  + Diagram would be helpful here

# Project Design and Implementation

* *including datapath, control unit, and any additional hardware/features*

# Evaluation Results

* *Max frequency of operation in simulation*
* *Percentage of chip area used in design*
* *Any other metrics*

# Discussion

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# Conclusion

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# Future Work

Due to the unfortunate cancellation of phases 3 and 4, there is much work to be addressed in the future. Specifically, the work that the team was able to complete did not include the Control Unit, and due to the closures of laboratories, it was not possible to implement the team’s code on an FPGA board. As such, the instructions *nop* and *halt* were not implemented but could be in the future.

# Appendix A: Code

*(insert all code here)*

# Appendix B: Simulation Results

*(snapshots of simulation results from phase 1 and 2)*

# Appendix C: Memory analysis of Phase 2

*(contents of memory before and after the program runs)*